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MODELS
PCIe-DIO-24HS
PCIe-DIO-24H

PCI Express 24 Channel Digital I/O Card with Change of State Detection

USER MANUAL

File: MPCIe-DIO-24HS.A1d

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ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A BOARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING BOARDS INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O BOARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

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If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

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Following Years: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

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Chapter 1: Introduction

The PCIe-DIO-24HS is a x1 lane PCI Express (PCIe) board designed for use in a variety of Digital I/O (DIO) applications. It uses the high speed PCIe bus to transfer digital data to and from the board. The DIO emulates 8255 compatible chips making it easy to program. This also allows for simple migration from older ACCES' PCI-based DIO boards. Change of State (COS) and interrupt capabilities relieve software from polling routines that consume valuable processing time. Lastly, the x1 lane PCIe connector is very flexible and can be inserted into any x1, x4, x8, x16, or x32 PCIe slots.

Features

- 24 high-current DIO lines
- 50-pin male header with ground lines on all even pins to suppress crosstalk
- COS interrupt ("S" models only)
- User interrupt on Port C bit 3
- DIO lines buffered
- Four and eight bit Ports independently selectable for inputs or outputs
- Pull-up resistors on DIO lines (user configurable pull-down)
- 5V VCCIO (3.3V user configurable)
- Fused VCCIO voltage available to the user on I/O header
- Compatible with industry standard I/O racks like Gordos, Opto-22, Potter & Brumfield, Western Reserve Controls, etc.

Applications

- Automatic test systems
- Laboratory automation
- Robotics
- Machine control
- Security systems, energy management
- Relay monitoring and control
- Parallel data transfer to PC
- Sensing switch closures or TTL, DTL, CMOS logic
- Driving indicator lights or recorders

Functional Description

This product is a x1 lane PCIe DIO board. It occupies sixteen bytes of I/O address space and the base address is selected by the system. The card emulates an 8255 compatible chip, providing 24 DIO lines in three 8-bit Ports: A, B, and C. Each 8-bit Port can be software configured to function as either inputs or outputs. Port C can be further broken into two 4-bit nybbles. Also, these nybbles can be software configured to function as either inputs or outputs.

This board has two methods for generating an interrupt. The first is using bit 3 of Port C (C3 IRQ). When this method is enabled, a rising signal edge detected on bit 3 of Port C will generate an interrupt. The second method uses COS detection hardware to produce an interrupt ('S' model only). When a Port has COS enabled, any changes of the Port's bits (low-to-high or high-to-low) will cause an interrupt. Refer to Chapter 5: Programming for enabling, disabling, and clearing the interrupts.

Each DIO line is buffered and capable of sourcing 32mA or sinking 64mA. The VCCIO level is 5V or can be configured as 3.3V.

By default, the DIO lines are pulled up with 10kΩ resistor networks to VCCIO. DIO lines can also be configured as pulled down by moving a jumper.

DIO wiring connections are via the 50-pin header on the mounting bracket of the board. This provides compatibility with OPTO-22, Gordos, Potter & Brumfield, and other module mounting racks. Every second conductor of the ribbon cable is grounded to minimize crosstalk between signals in the cables. VCCIO is available on each I/O connector (pin 49) for external use, see page 10.

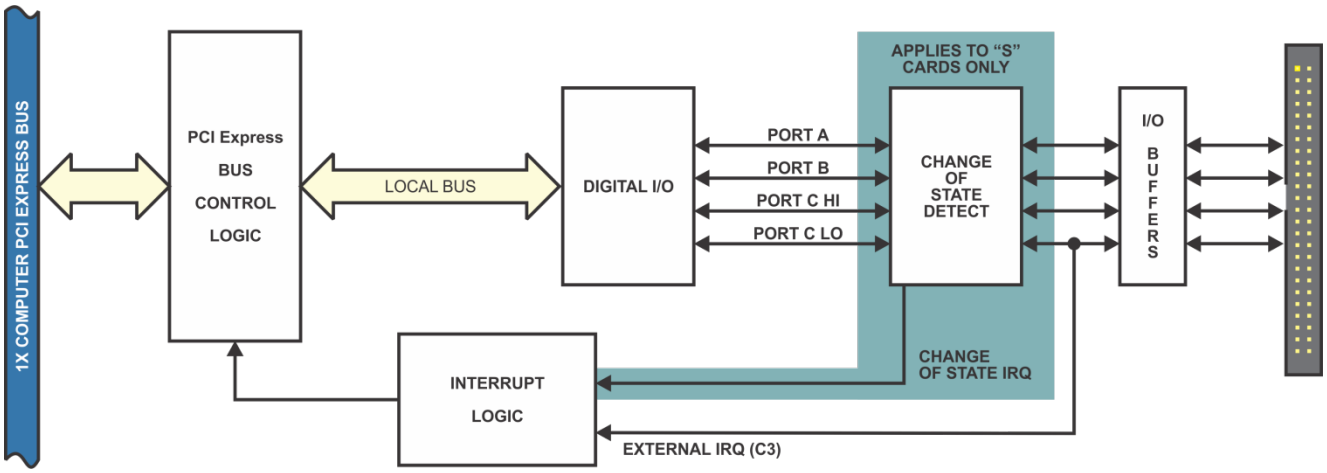

Figure 1-1: Block Diagram

Ordering Guide

- PCIe-DIO-24HS 24-bit Digital I/O card with change of state detection, with a latching 50 pin header on the card mounting bracket
- PCIe-DIO-24H 24-bit Digital I/O card with a latching 50 pin header
- PCIe-DIO-24HS-S01 24-bit Digital I/O card with change of state detection, non-latching 50 pin connector, & quick disconnect grounding tab on the mounting bracket

Factory Options

- Extended temperature operation (-40° to +85°C)
- RoHS compliant version

Optional Accessories

• CAB50F-6	Six-foot ribbon cable assembly with 50-pin female connectors	
• CAB50-6	Six-foot ribbon cable assembly with a 50-pin female header connector and a 50-pin female edge connector	
• STB-50	Screw terminal board, ships with standoffs but can also mount on SNAP-TRACK or DIN-SNAP	
• DIN-SNAP-6	Six inch length of SNAP-TRACK with two clips for mounting an STB-50 screw terminal board on a DIN rail	

Table 1-1: Accessories

Chapter 2: Installation

Software CD Installation

The software provided with this board is contained on one CD and ***must be installed onto your hard disk prior to use.*** To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your drive where you see D: in the examples below.

Windows

a. Place the CD into your CD-ROM drive.
b. The install program automatically run. If the install program does not run, click START | RUN and type D:\INSTALL, click OK or press Enter.
c. Follow the on-screen prompts to install the software for this board.

Linux

a. Please refer to linux.htm on the CD for information on installing under Linux.

Hardware Installation

Please install the software package before plugging the hardware into the system.
Refer to the printed I/O Quick Start Guide included with your board which can also be found on the CD, for specific, quick steps, to complete the hardware and software installation.

Caution! ESD

A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.

Chapter 3: Hardware Details

Option Selection

Refer to the setup program on the CD provided with the board. Also, refer to the Block Diagram and the Option Selection Map when reading this section of the manual.

VCC Select

Position the jumper to select either 5VTTL logic, or 3.3VDC logic.

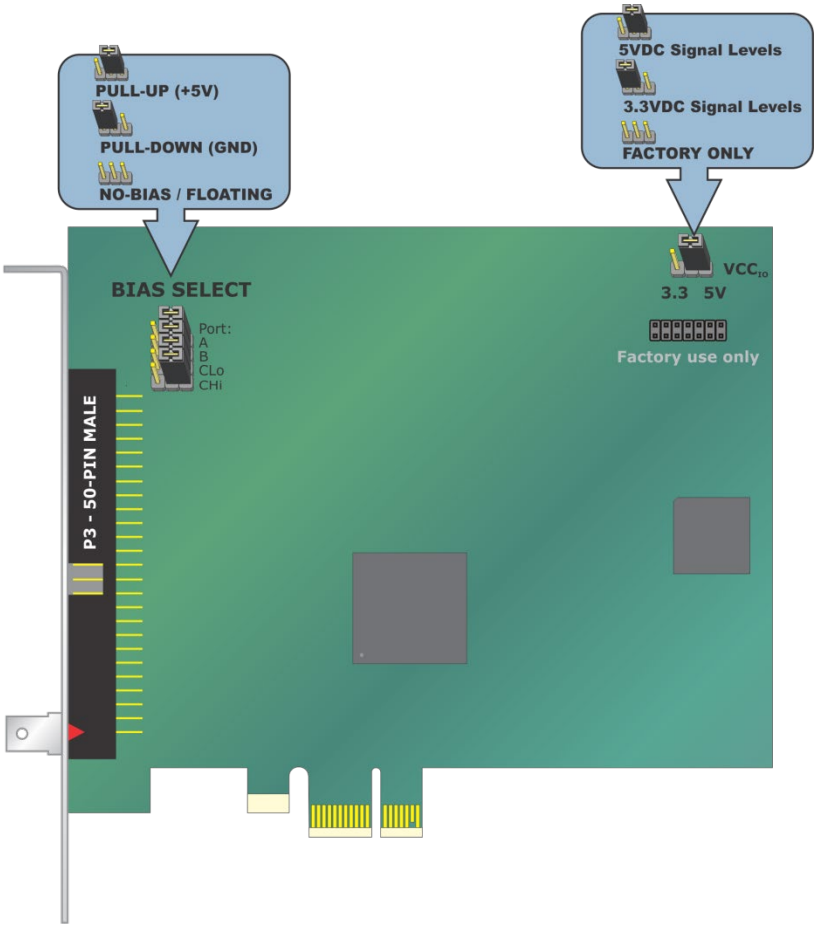

Figure 3-1: Option Selection Map

Bias Select

Select 10k ohm pull up or pull down resistors per port using the provided jumpers on the card.

50 Pin Header

The latching 50 pin header has standard 0.100" spacing between pins and is keyed to prevent improper connections. It can be used with standard IDC type ribbon cables. A non-latching header is used for the –S01 card version.

Quick-Disconnect Grounding Tab

A quick disconnect grounding tab exists on the mounting bracket for the –S01 card version. It is connected to the board ground plane, which connects to the PC power supply return / chassis ground.

VCCIO Resettable Fused Output

There is a 0.5A resettable fuse. It connects to pin 49 of the I/O connector and is used to protect the card and PC power supply when used to power external module racks, relay boards, or for general purposes. If an over-current persists on a circuit protected by the resettable fuse, it will open interrupting power to the circuit. The amount of time it takes the fuse to act depends on the amount of over-current and other conditions such as ambient temperature, humidity, etc. The fuse will remain open until the bi-metal elements cool sufficiently, at which time the circuit will be restored.

Chapter 4: Address Selection

The Vendor ID for this card is 0x494F. (ASCII for "IO")
The Device ID for the PCIe-DIO-24HS is 0x0E54.
The Device ID for the PCIe-DIO-24H is 0x0C53.

This card uses I/O addresses offset from the base address assigned by the PCIe bus. The address spaces are defined in the programming section of this manual.

PCIe architecture is Plug-and-Play. This means that the BIOS or Operating System determines the resources assigned to PCIe cards rather than the user selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

The following information is for advanced users only:

The PCIe bus supPorts 64K of I/O address space, so your card's addresses may be located anywhere in the 0000h to FFFFh range.

To determine the base address that has been assigned, run the PCIFind utility program. This utility will display a list of all the cards detected on the PCI/PCIe bus, the addresses assigned to each function on each of the cards, and the respective IRQs.

Alternatively, Windows systems can be queried to determine which resources were assigned. In these operating systems, you can use either PCIFind, or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

In Linux you can use the LSPCI command to determine this information. A PCIFind.pl script is also provided which may simplify this task.

An example of how to locate PCIe card resources in DOS is provided with in the PCI\SOURCE directory, under your installation directory. This code runs in DOS, and uses the PCI defined interrupt BIOS calls to query the PCI bus for card specific information. You will need the Device ID and Vendor ID listed above to use this code.

The card uses more resources than you usually need be concerned with. PCIFind will show only the most commonly required information to reduce confusion.

For those who require it, be aware of the following:
BAR[0]: memory mapped, IRQ Status bit
BAR[1]: I/O mapped, reserved
BAR[2]: I/O mapped card registers (← all most software needs)

Chapter 5: Programming

This card is an I/O-mapped device that is easily configured from any language. The base address is assigned by the computer system during installation. The card's read/write functions are as follows.

Address	Function	Operation
Base Address +0	Port A	Read/Write
Base Address +1	Port B	Read/Write
Base Address +2	Port C	Read Write
Base Address +3	Control Register	Read/Write
Base Address +4 through +9	Not used	N/A
Base Address +A	DIO Buffer Enable	Read/Write
Base Address +B	DIO COS IRQ Enable (S Models Only)	Read/Write
Base Address +C	Not used	N/A
Base Address +D	Global IRQ Disable	Write
Base Address +E	Port C bit-3 IRQ Enable	Read/Write
Base Address +F	IRQ Clear	Write

Table 5-1: Register Address Map

Base Address +0 (read/write) Port A DIO

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

Table 5-2: Base +0 Port A DIO

Reading from this address will return the digital data on Port A. Writing to this address will output the digital data on Port A. Readback is supported while in output mode. Base Address +3 controls Port A's input/output direction.

Base Address +1 (read/write) Port B DIO

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

Table 5-3: Base +1 Port B DIO

Reading from this address will return the digital data on Port B. Writing to this address will output the digital data on Port B. Readback is supported while in output mode. Base Address +3 controls Port B's input/output direction.

Base Address +2 (read/write) Port C DIO

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Table 5-4: Base +2 Port C DIO

Reading from this address will return the digital data on Port C. Writing to this address will output the digital data on Port C. Readback is supported while in output mode. Port C can also be broken into two nybbles, Port C Low (bits 0-3), and Port C High (bits 4-7). Each nybble can be independently set as input or output. Base Address +3 controls Port C's I/O direction.

Base Address +3 (read/write) Control Register

The DIO function contains a control register. This 8-bit register is used to set the direction of the Ports. At power-up or reset, all DIO lines are automatically set as inputs and should be configured during initialization by writing to the control register even if the Ports are going to be used as inputs. Bit 7 must be set to '1' when configuring the direction of the Ports. This register can be readback with bits 2, 5, 6, always reading zero, and bit 7 always reading one.

Ports can be written to while configured as inputs. When a Port is changed from input to output, the last written value will be applied. If a Port has never been written to, the value on the Port's pins while in input mode will be applied to the Port when configured as an output. This prevents the Ports pins from glitching when set as outputs.

Bit	Assignment	Code
D0	Port C Lo (C0-C3)	1=Input, 0=Output
D1	Port B	1=Input, 0=Output
D2	Reserved	Set to '0'
D3	Port C Hi (C4-C7)	1=Input, 0=Output
D4	Port A	1=Input, 0=Output
D5,D6	Reserved	Set to "00"
D7	Direction Set Flag	1=Active

Table 5-5: Base +3, DIO Port Direction Control Register

Base Address +4 through +9 Not Used

Base Address +A (read/write) DIO Buffer Enable / Disable (tri-state)

At power-up or reset, all DIO buffers on the card are enabled. To globally disable the DIO buffers write a one to bit 0. To globally re-enable the DIO buffers, write a zero to bit 0. When the buffers are disabled the connector pins are tri-stated and biased by the state of the pull up or down configuration jumper. A read returns the buffer status; 0=enabled, 1=disabled.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	'0'	'0'	'0'	Port A	Port C Hi	'0'	Port B	Port C Lo
Write	unused							Disable

Table 5-6: Base +A, DIO Buffer Enable Read / Write

Base Address +B (read/write) IRQ Enable DIO COS (S models) and C3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
'0'	'0'	'0'	'0'	'0'	Port C	Port B	Port A

Table 5-7: Base +B, IRQ Enable COS and C3

At power-up or reset, all IRQ sources on the card are disabled. To enable the COS IRQ, write a zero to the bits that correspond to the port(s) desired. Any changes detected on the bits within the enabled port(s) will generate an IRQ. To disable COS IRQ, write a one to bits that correspond to the port(s) desired.

Base Address +C Not Used

Base Address +D (write) IRQ Disable Global

Write any value to this address to disable all IRQ sources on the card.

Base Address +E (read/write) IRQ Enable Port C bit-3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
'0'	'0'	'IRQ Output'	'1'	'0'	'0'	'0'	C3

Table 5-8: Base +E, Port C3 IRQ Enable

At power-up or reset, all IRQ sources on the card are disabled.

To enable the C3 IRQ, write a one to bit 0. A rising edge detected on bit 3 of Port C will generate an IRQ. To disable the C3 IRQ, write a zero to bit 0.

Bit 4 is a read-only, and is always a '1' to maintain backwards compatibility with the PCIe-DIO-24DS.

Bit 5 is a read-only, which is the status of the board IRQ output pin. A "1" indicates the IRQ is active (latched). A "0" indicates no IRQ is pending.

Base Address +F (write) IRQ Clear

Any value written to this address will clear the status bit and pending IRQ.

Chapter 6: Connector Pin Assignments

A 50-pin male header is provided for I/O connection. The mating connector is an AMP type 1-746285-0 or equivalent

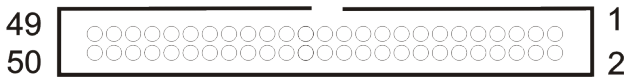

Figure 6-1: 50-Pin Male Header

Pin	Signal Name	Pin	Signal Name
1	PC7	2	GND
3	PC6	4	GND
5	PC5	6	GND
7	PC4	8	GND
9	PC3*	10	GND
11	PC2	12	GND
13	PC1	14	GND
15	PC0	16	GND
17	PB7	18	GND
19	PB6	20	GND
21	PB5	22	GND
23	PB4	24	GND
25	PB3	26	GND
27	PB2	28	GND
29	PB1	30	GND
31	PB0	32	GND
33	PA7	34	GND
35	PA6	36	GND
37	PA5	38	GND
39	PA4	40	GND
41	PA3	42	GND
43	PA2	44	GND
45	PA1	46	GND
47	PA0	48	GND
49	VCCIO	50	GND

Table 6-1: Connector Pin Assignments

* This line is an I/O Port and also used for C3 IRQ.

Signal Name	I/O	Signal Description Name
PC7	I/O	Port C bit 7
PC6	I/O	Port C bit 6
PC5	I/O	Port C bit 5
PC4	I/O	Port C bit 4
PC3	I/O	Port C bit 3 / when C3 IRQ is enabled will generate an IRQ on a rising edge
PC2	I/O	Port C bit 2
PC1	I/O	Port C bit 1
PC0	I/O	Port C bit 0
PB7	I/O	Port B bit 7
PB6	I/O	Port B bit 6
PB5	I/O	Port B bit 5
PB4	I/O	Port B bit 4
PB3	I/O	Port B bit 3
PB2	I/O	Port B bit 2
PB1	I/O	Port B bit 1
PB0	I/O	Port B bit 0
PA7	I/O	Port A bit 7
PA6	I/O	Port A bit 6
PA5	I/O	Port A bit 5
PA4	I/O	Port A bit 4
PA3	I/O	Port A bit 3
PA2	I/O	Port A bit 2
PA1	I/O	Port A bit 1
PA0	I/O	Port A bit 0
VCCIO	O	5V or optionally 3.3V via 0.5A resettable fuse for external module racks etc.
GND	X	Ground

Table 6-2: I/O Header Connector Signal Names, Directions and Descriptions

Chapter 7: Specifications

VCCIO 5V or 3.3V (jumper configurable)

Logic Levels	5V		3.3V	
Low Inputs	≤ 1.5V	≤ 2uA	≤ 0.8V	≤ 2uA
High Inputs	≥ 3.5V	≤ 2uA	≥ 2.0V	≤ 2uA
Low Outputs	≤ 0.55V	32mA	≤ 0.55V	24mA
High Outputs	≥ 3.8V	32mA	≥ 2.4V	24mA

Table 7-1: VCCIO Logic Levels

Power Output VCCIO (P3 pin 49)

Environmental

Operating Temperature 0° to 70°C, optional -40° to +85°C

Storage Temperature -55° to +150°C

Humidity 5% to 95% RH, without condensation

Board Dimensions Length - 6.6"; Height - 4.2" (seated)

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com***. Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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